Abstract OF THE DISCLOSURE

A first-in-first-out (FIFO) module is disclosed. The FIFO module includes multiple individually addressable memory locations, a write pointer, a read pointer and at least additional pointer. The write pointer is connected to the memory bank for addressing a first memory location to write a datum on an input data bus into the first memory location. The read pointer is connected to the memory bank for addressing a second memory location to read a datum stored therein onto an output data bus. The at least one additional pointer is connected to the memory bank for addressing a third memory location to read a datum stored therein. A deskew circuit and a rate matching circuit which utilize the FIFO module, and a deskew method are also disclosed.